Heterojunction Silicon Microwire Solar Cells

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S *Supporting Information*

ABSTRACT: We report radial heterojunction solar cells of amorphous silicon on crystalline silicon microwires with high surface passivation. While the shortened collection path is exploited to increase the photocurrent, proper choice of the wire radius and the highly passivated surface prevent drastic decrease in the voltage due to high surface-to-volume ratio. The heterojunction is formed by depositing a ~12−16 nm of amorphous silicon on crystalline silicon wires of radius approximately equal to minority carrier diffusion length (~10 μm). In spite of very short carrier lifetime (<1 μs), the microwire array devices generate photocurrent of ~30 mA/cm^2, and the same time, voltages close to 600 mV are achieved, leading to efficiency in excess of 12% in extremely short carrier lifetime silicon. We also find that formation of nanocrystallites of silicon in the deposited film results in loss of the expected passivation.

KEYWORDS: Solar cells, silicon heterojunction, radial junction, silicon microwire, surface passivation
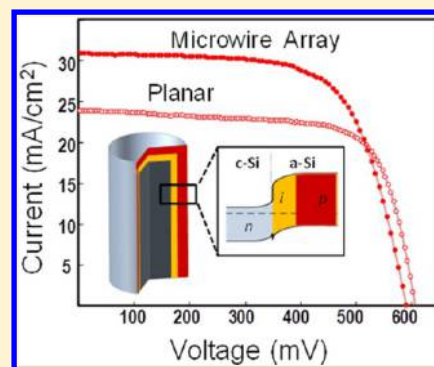
Radial pn junction silicon devices have been extensively considered for solar cell applications due to the potential for superior optical and electronic performance. Vertically aligned wires are known for strong broadband absorption.[1−6] The effect can be attributed to reduced reflection due to nanotexturing as well as enhanced optical path length of guided mode couplings. These optical properties create a possibility for using thinner layers and thus less material in silicon solar cells. From the electronic viewpoint, the vertical junction of the radial diode provides a collection path separated from the photon absorption thickness; while photons are absorbed along the height of the wires, carriers are collected along the radial direction.[6,7] Thus, in wires with small radius sizes, photo-generated carriers can diffuse to the junction with minimal recombination. This latter feature has the potential to enable the utilization of lower quality material, in which high density of impurities and defects leads to short minority carrier life-time[7,8]—materials that would normally result in low efficiency in planar structures. Although the potential advantages of the radial pn junction structure have inspired a number of studies on silicon wire solar cells,[9−21] there are still key aspects to be considered and design challenges yet to be addressed in order to exploit these advantages in practice. In particular, lower open circuit voltages (V_{oc}) are obtained in wire solar cells in spite of higher short circuit current (I_{sc}), which is due to higher saturation current across the increased junction area. We report, in this paper, a radial pn heterojunction cell and demonstrate that by appropriate choice of the size according to the quality of the start material at hand, and by employing a highly passivating heterojunction structure, high voltage and current can be obtained simultaneously, resulting in increased cell efficiency in extremely low quality silicon material.

For the radial junction wire cell design to achieve maximum potential efficiency, appropriate choice of the wire size is critical. The increase in photocurrent due to efficient radial carrier diffusion at smaller radii saturates when wire radius is approximately equal to the diffusion length.[7] At this scale, the effect of dark current dominates the cell behavior; rapid increase in the saturation current of thinner wires drastically reduces the voltage.[8] The optimal radius is in fact of the order of the minority carrier diffusion length. In the case of crystalline silicon, even with high density of defects and deep level traps, the diffusion length often remains in the micrometer range. For instance, under extreme conditions of 10 ns carrier lifetime and 1 cm^2/s diffusion coefficient, the diffusion length is still 1 μm. Given the steep increase in the saturation current for wire radii smaller than diffusion length,[8] nanoscale Si wire radial pn junction design will always suffer from dramatically degraded voltage.[9,21] Moreover, micrometer size wire design will be beneficial only for start material with very short diffusion length.[15]

In addition to the essential design criteria of wire radius for a specific material quality, it is also necessary to minimize the saturation current of the junction in order to achieve high

voltage. With the increased area of the vertical junction, the saturation current is greatly affected by junction characteristics and the surface recombination at the outer wall of the wire.[8] Heterojunction of crystalline silicon (c-Si) and wider bandgap amorphous silicon (a-Si) with a thin intrinsic layer in between, known as HIT structure pioneered by Sanyo,[22] is recognized to result in cells with very low saturation current. The structure consists of n-type crystalline base and p-type amorphous emitter layer, with an intrinsic a-Si layer in between. The thin intrinsic interlayer leads to very low density of interface states, which passivates the surface to form a high quality junction. At the same time, the equilibrium Fermi level alignment of p-type a-Si on n-type c-Si creates a band offset that inhibits the approach of the carriers to the surface,[22,23] creating a minority carrier "mirror", thus suppressing the saturation current.[24,25]

The radial pn heterojunction cell is depicted in Figure 1. It consists of n-type c-Si core with radius approximately equal to
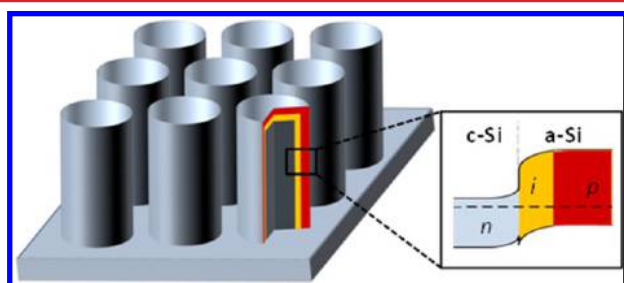
Figure 1. Schematic of the heterojunction microwire array solar cell. The core is n-type crystalline silicon, and the shell consists of a bilayer stack of intrinsic and p-type amorphous silicon; the right panel represents the band structure of the heterojunction.

the diffusion length of the start material and p-type a-Si layer as the emitter. The keys to achieving the high voltage are the higher bandgap, passivating layer,[26] and the appropriate choice of the wire radius.[8] It has been shown theoretically[27] and experimentally[28] that the band offsets in the p-type a-Si/n-type c-Si structure result in better passivation and efforts to duplicate the performance on p-type wafer have led to inferior open circuit voltages.[29] We used two start n-type wafers from different quality single crystal upgraded metallurgical grade (UMG) silicon with 0.1 Ω·cm resistivity and ∼200 μm thickness. The diffusion lengths were determined to be approximately 7.9 and 15 μm in the two samples (named A and B, respectively) from minority carrier lifetime measurements shown in the Supporting Information. 5 mm × 5 mm microwire array cells with radii ranging from 1.5 to 50 μm were fabricated on each of the start wafers. Figure 2a shows scanning electron microscope (SEM) images of a sample microwire array. The wire areas were defined by photolithography on the top surface of the substrates, and wires of 22 μm height were etched using deep reactive ion etching (DRIE) in arrays with hexagonal unit cell. The filling fractions of wires on the surface for the results reported here are 50%; i.e., the center-to-center distance of the wires is ∼2.7 times their radius. Planar cells with the same area but without microwires were also included within the lithography mask to produce planar junction devices for control experiments. After DRIE, the structures bear a considerable surface damage and contamination. Depositing a-Si on the as processed microwires led to shunted devices or cells with very low open circuit voltages (<200 mV). The samples underwent a rigorous cleaning process to remove the
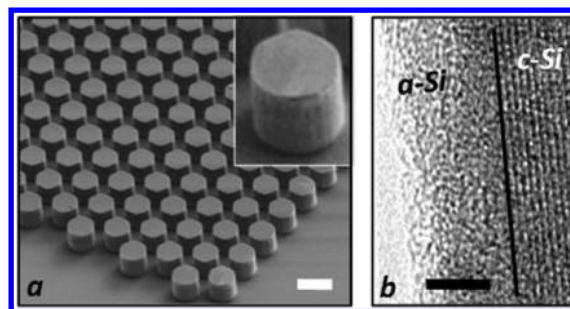

Figure 2. (a) SEM image of the Si microwire array, fabricated using deep reactive ion etching, after cleaning and deposition of amorphous silicon; the inset is the magnified image of a single microwire with ∼22 μm height and 10 μm radius. (b) TEM image of the amorphous−crystalline heterojunction, showing a thoroughly amorphous phase deposition. Scale bars are 30 μm and 5 nm in panels a and b, respectively.

damage from the surface (as seen in the Supporting Information), which was found to be extremely critical in obtaining high quality surface for deposition of a-Si for high efficiency cells.

The a-Si layers were deposited using plasma enhanced chemical vapor deposition (PECVD) at <150 °C (details in the Supporting Information). Figure 2b shows transmission electron microscopy (TEM) image of the a-Si layer on a c-Si microwire. To establish the passivation effect of the films, we simultaneously deposited the same films on high quality single crystal Czochralski planar wafers with bulk carrier lifetime of more than 100 μs. We then measured the "apparent" carrier lifetime after a-Si PECVD, which represents the passivation quality (see Supporting Information). It was found that controlling the deposition temperature was critical in achieving maximum passivation of c-Si, and higher temperature led to a drastic decrease in the apparent lifetime as shown in Figure 3. Limiting the deposition temperature is the key to obtaining fully amorphous structure[30] which is required for the passivating heterojuction. Higher temperature deposition results in (partial) crystallization of the film into a mixture of amorphous phase and silicon nanocrystallites, in which the passivation starts to fade away.[31] This can be explained by the observed drop in the film bandgap when transitioning from fully amorphous to nanocrystalline structure, for which the bandgap emerges at close to c-Si gap (1.1 eV).[32] In this case, the band offsets required for the minority carrier mirror effect practically disappear, and the device experiences operation similar to a diffused homojunction with high saturation current. Such cells would need an actual passivation layer such as silicon nitride[20] and will only produce acceptable efficiencies in sparse wire arrays, which are not appropriate for low quality start material.

Prior to a-Si deposition, the surface of the cells was wetted with hydrogen in the plasma chamber to provide a high quality interface. The film thicknesses were slightly higher on the horizontal surfaces than on vertical wire walls due to difference in deposition rate. The total thicknesses of the a-Si bilayers were approximately 12−16 nm (4−6 nm for the intrinsic layer and 8−10 nm for the doped layer); images from different spots along the interface revealed the uniformity of the amorphous deposition in PECVD. Thicker films significantly degrade the blue response and the photocurrent due to strong photon absorption in the a-Si, where carrier collection is inefficient. The low thermal budget process of depositing a-Si layer on c-Si,
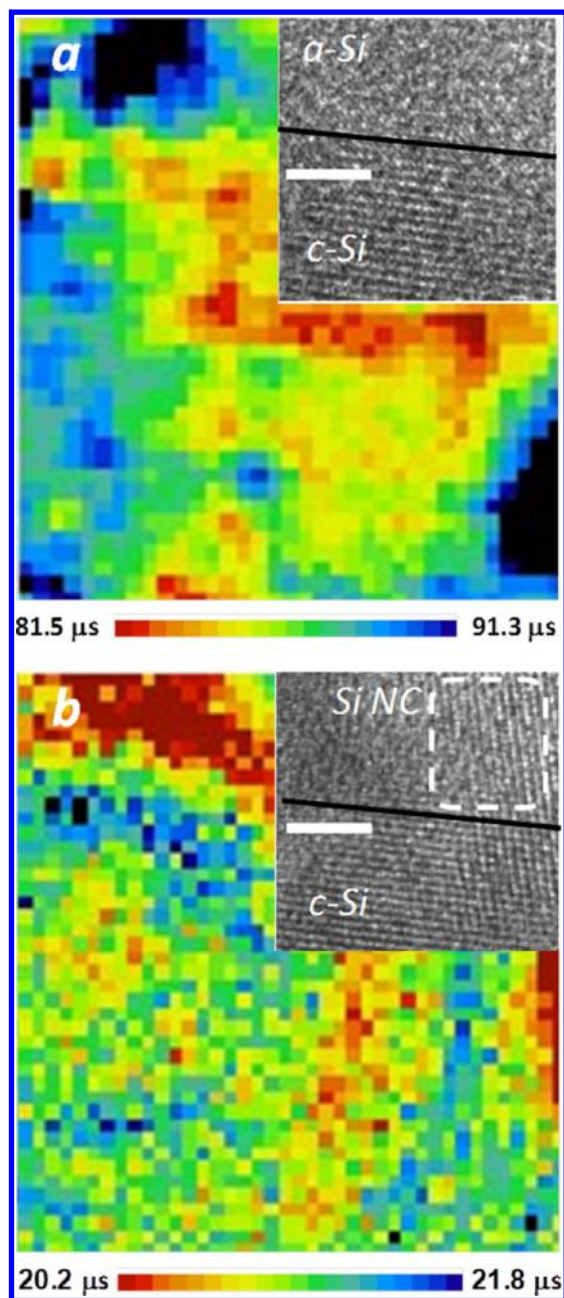
Figure 3. Maps of measured apparent lifetime (reflecting surface passivation quality) for heterojunction film deposition at (a) 140 °C and (b) 180 °C on planar high quality control wafers; insets show TEM images of the interface. A fully amorphous phase results in high measured apparent lifetime. Lifetime drops as passivation vanishes when silicon nanocrystallites (Si NC) start to form at higher deposition temperature. The area of the lifetime map is ∼2 × 2 cm, and the scale bars are 5 nm for TEM insets.

were sputtered as the front transparent conductive oxide (TCO) and the back-contact of the device.

The performance of the fabricated cells was characterized by spectral response and AM1.5 illuminated current voltage (I−V) measurements. All microwire cells, irrespective of the radius size, showed a higher short circuit current compared to the control planar heterojunctions. On the other hand, lower open circuit voltages were consistently obtained with decreasing wire radius sizes. The highest efficiency was obtained for wire radius sizes of 10 and 15 μm respectively for the start wafers A and B. Figure 4 shows the solar cell measurement results of these
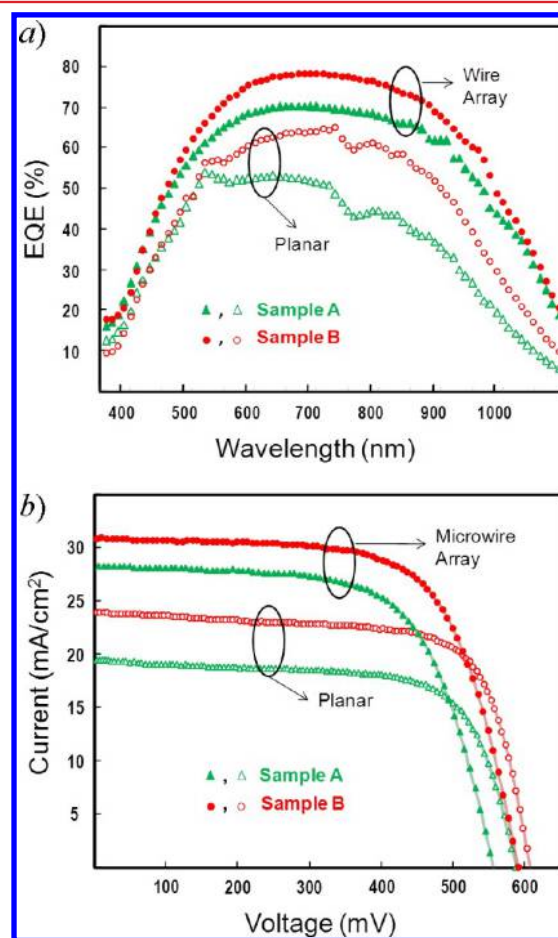
Figure 4. Measured external quantum efficiency (a) and illuminated current voltage characteristics (b) of the planar and microwire array cells on start wafers A and B; wire sizes are 10 and 15 μm for A and B, respectively. The microwire array cells have a stronger spectral response and generate larger photocurrent due to more efficient carrier collection in the vertical junction. The heterojunction structure also prevents drastic reduction in the open circuit voltage as a result of surface area increase.

while a fabrication advantage, in general, could be of particular interest in the case of lower purity and high defect silicon material, as it may avoid the possibility of defect activation after prolonged high temperature excursion. We also found the fabricated devices in this particular case showed no sensitivity to the back passivation that is present in a standard HIT device,[22] which is due to the short carrier diffusion length in the start material compared to the wafer thickness. Finally, 200 nm aluminum doped zinc oxide (AZO) and 800 nm aluminum

microwire array cells as well as those of the planar cells on the same start wafer. Comparison of the external quantum efficiency (EQE) of the microwire cells versus planar cells confirms the effectiveness of the radial junction for compensating the short minority carrier lifetime of the start material. The microwire cells show much stronger response in the longer wavelength part of the spectrum. It must be noted that the shorter wavelength response of the cells is dominated by strong absorption of high energy photons in the TCO and a-Si window layers. We also note that a smaller fraction of the

increase in EQE is due to reduced reflection at the not perfectly horizontal and vertical surfaces created after DRIE and cleaning, causing multiple incidences.[15] This is however much less prominent than the effect of radial carrier collection in this case. The strong spectral response of the microwire cells results in the greater short circuit current (∼30 mA/cm²) obtained in the microwire devices. Interestingly, the increased surface area of the microwire devices compared to the planar devices does not entail significantly lower open circuit voltage, which is made possible by the small saturation current of the heterojunction. In addition to the highly passivated structure, the appropriate choice of the radius minimizes the effect of surface recombination on the saturation current. At the same time, the enhancement in the photocurrent partially compensates the inevitable increase in the saturation current. As a result, the open circuit decreases by only 20−30 mV due to the increase in surface area. The measured parameters of the cells made on start wafers A and B are summarized in Table 1 for the planar

Table 1. Measured Cell Parameters under AM1.5 Irradiance for the Planar and Microwire Array Heterojunction Devices on the Two Start Wafers A and B

	J (mA/cm²)	V (mV)	fill factor	efficiency (%)
sample A planar	19.4	588	0.695	7.93
sample B planar	23.9	608	0.709	10.31
sample A microwire array	28.6	557	0.645	10.27
sample B microwire array	31.1	591	0.664	12.20

and microwire array devices. Implementing the heterojunction microwire array structure on each of the start wafers results in an efficiency improvement of ∼2% absolute; in spite of the very low carrier lifetime (<1 μs), efficiency exceeding 12% was achieved. A major source of losses in the devices was identified to be the front contact TCO. The high sheet resistance of the 200 nm film affects the fill factor of the devices. This is primarily due to the low temperature deposition of AZO, which is necessary to preserve the a-Si film properties. While thicker AZO (600 nm) was found effective in reducing the series resistance and also forming a fully conformal contact layer along the wire sidewalls, it resulted in drastically reduced current due to considerably lower transparency compared to high temperature deposited AZO (∼50% for the 600 nm film).

Although the wires are relatively closely packed, a significant part of the response in the microwire array cell is obtained from the planar regions of the wafer between the wires (50% of the cell area is covered by wires and the remaining is planar "background"). Laser mapping of the photocurrent of the devices (see Supporting Information) shows that the radial junction indeed improves the current considerably. To accurately differentiate the response from the microwires and the background, we performed spatially resolved measurements of the cell response using a focused laser beam at three different wavelengths of 488, 650, and 850 nm. The normalized photoresponse in Figure 5 shows that microwire regions generally have a stronger response particularly at 850 nm excitation, where photons penetrate deeper into the material. The planar regions of the array device area also show slightly higher photoresponse than a planar cell due to reduction in the reflection; the effect from nonperfect profile of the vertical and horizontal etched surfaces appears less prominently in the case of laser excitation.
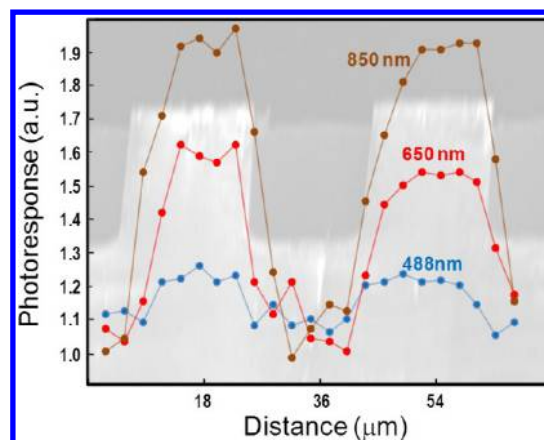
Figure 5. Normalized spatially resolved photoresponse of the microwire array device (from sample A), for three different laser excitation; the SEM of the laser scanned path is displayed in the background to show the approximate location of each reading point. The wires (vertical junction areas) generate considerably stronger photocurrent compared to the areas between wires (planar junction areas); the longer wavelength benefits more from the enhanced carrier collection efficiency. In order to enable resolving the photoresponse in the regions between the wires, a lower areal density microwire array (25% filling fraction) was used for this measurement.

In conclusion, we showed radial heterojunction devices with high efficiencies (∼12%) on extremely low quality silicon material (carrier lifetime <1 μs). The achieved high efficiency is made possible by (a) efficient carrier collection in the radial junction, (b) appropriate choice of the wire radius to optimize the carrier collection versus surface area increase, and (c) high quality passivation in the a-Si/c-Si heterojunction, in addition to the reduced surface reflectivity of the microwire arrays. Although the demonstrated device is based on top-down etching of lithographically defined wires, the design can be implemented on bottom-up grown wires as well. Thus, the proposed device can enable cost-effective and efficient use of material for solar cell fabrication through reducing the material consumption per cell area (in the case of bottom-up grown wires) and utilization of inexpensive feedstock (in the case of low grade silicon wafers).

■ ASSOCIATED CONTENT

Ⓢ Supporting Information
Experimental details; Figures S-1−S-3. This material is available free of charge via the Internet at http://pubs.acs.org.

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■ ACKNOWLEDGMENTS

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